Prelab Assignment
Experiment 3
ECE 482

Fig. 1 shows the power stage of the drivetrain boost converter assembled in experiment 2 along with the closed loop control and compensation circuitry to be implemented in experiment 3. For all parts of this prelab, consider operation of the boost converter with the following:

- V_{bat} = 26 V
- V_{bus} = 50 V
- 0 W < P_{out} < 250 W

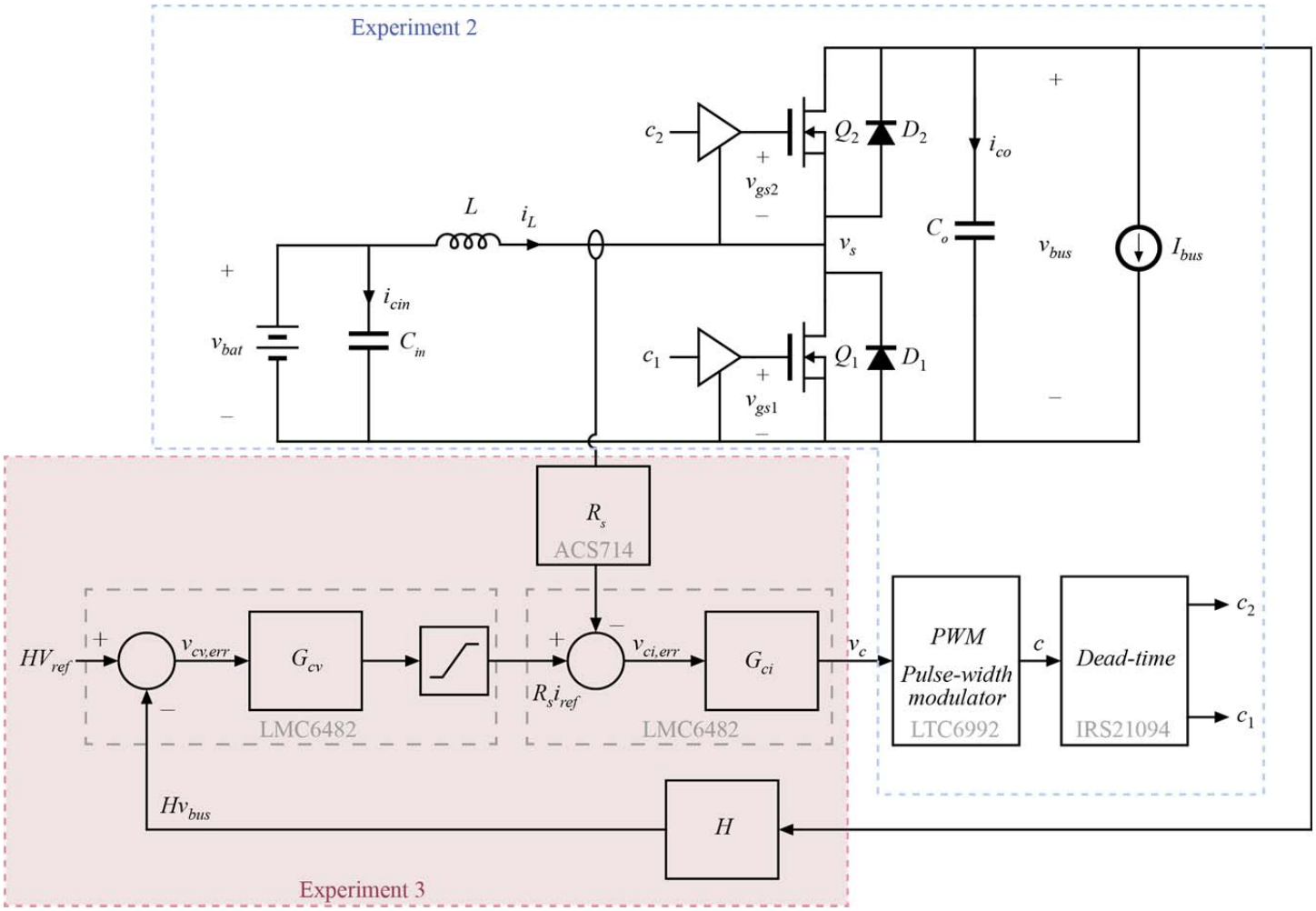

Figure 1: Closed-Loop Boost Converter

Part 1: Solving Boost Transfer Functions

Solve the following (open-loop) transfer functions of your power stage, as realized in experiment 2:

$$G_{id}(s) = \left.\frac{\hat{i}_l}{\hat{d}}\right|_{\hat{v}_{bat}=0,\hat{i}_{bus}=0} \qquad G_{vi}(s) = \left.\frac{\hat{v}_{bus}}{\hat{i}_l}\right|_{\hat{v}_{bat}=0,\hat{i}_{bus}=0}$$

Based on your intuition from experiment 2, include any parasitic elements which you suspect may significantly affect the dynamic behavior of the circuit. Model the output port as a current source, I_{bus}, whose value may be either positive or negative depending on the direction of power flow.

Part 2: Boost Compensator Design

A small-signal block diagram of the closed-loop boost is given in Fig. 2. Note the locations of the transfer functions solved in Part 1, and the correspondence between Figs. 1 and 2.

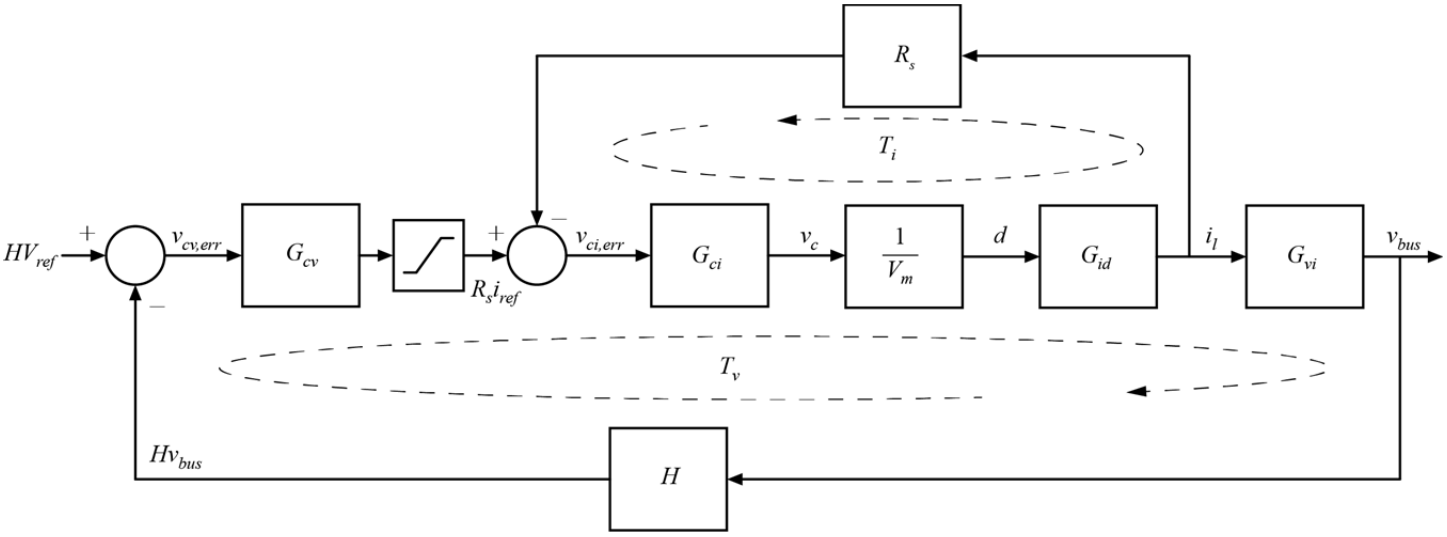

Figure 2: Small-Signal block diagram of closed-loop boost converter

You may assume for now that $R_s = 1$, $V_m = 1$, and $H = 1$ (you will solve/design these later). Design the current and voltage compensators, G_{ci} and G_{cv} to obtain well-behaved closed-loop operation of the converter. That is, select the DC gain as well as the number and frequency of poles and zeros in each so that the loop gains of both current and voltage control loops are stable, fast, and exhibit low overshoot. You will need to make tradeoffs between each of these characteristics, but keep the following in mind:

- All crossover frequencies and closed-loop bandwidths must be well below the switching frequency of the converter
- Low gains are desired at frequencies at and above the switching frequency in order to attenuate switching noise
- In general, the current control loop should have a much higher bandwidth than the voltage control loop
- High (or infinite) DC gain is desired so that the control loops will accurately track their references in steady state
- $\varphi_m > 0$ is required for stability, but larger phase margin is desirable to reduce overshoot and ringing (see Fig. 3)

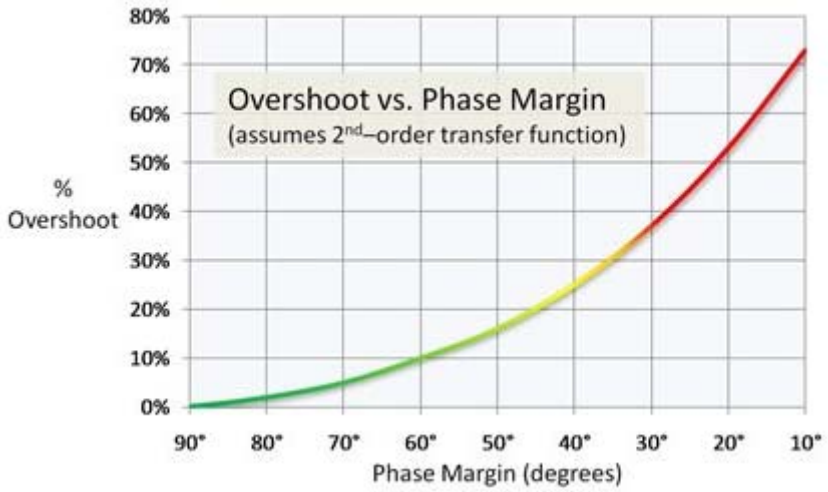

Figure 3: Relation between overshoot in response to a step input and phase margin of a dominantly 2nd-order transfer function

Turn in bode plots of the loop gains T_v and T_i in your current and voltage control loops for a variety of operating points spanning the range of power levels in each power flow direction. Additionally, turn in plots of the closed-loop step response from voltage reference to bus voltage at these same operating points.

Part 3: Compensator Realization

Fig. 4 shows an example op-amp circuit capable of realizing a generic PID compensator. Depending on the design of your compensators from the previous section, this circuit may be appropriate for realizing the transfer functions you designed in Part 2. If your compensator is less complex, you may remove passive elements as necessary.

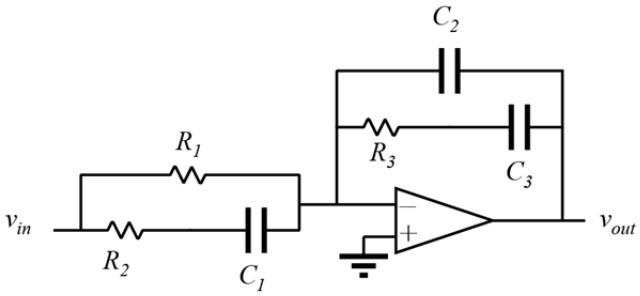

Figure 4: Op-amp compensation circuit

Starting from the circuit of Fig. 4 using the graphical analysis techniques discussed in class or any other design approach, select values for the resistances and capacitances to realize your transfer functions G_{ci} and G_{cv}.